REMARKS/ARGUMENTS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

Applicant respectfully requests acknowledgment that the certified copies have been received as this is a divisional application, and certified copies have been previously submitted and received in the parent application.

Claims 5, 7, 9, 10, 12, and 14 have been amended due to informalities and to correct the incorrect expressions. Claim 15 has been added.

Claims 9 and 12 are objected to because of informalities. Claim 12 has been amended to correct the informality as requested by the examiner. Claim 9 was previously amended in line 14 using double brackets to delete the character "s" in the word "terminals". The use of double brackets in this situation is allowed, per the revised amendment practice, since the amendment was for the deletion of five characters or fewer. Therefore, the word "terminals" has not been changed in claim 9.

Claims 5 and 7-9 stand rejected under 35 U.S.C. 102(b) as being anticipated by Iida (U.S. Patent No. 5,500,542). For at least the following reasons, the examiner's rejection is respectfully traversed.

Iida does not disclose or teach that "the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks" as recited in claim 5. Similar language is found in claims 7 and 9.

Iida discloses a diode connected between the gate and the substrate of a pMOS transistor

(col. 1, lines 40-45; Figs. 28A, 28B and 29). Iida also discloses that wiring connecting two cells passes through a diode (see Figs. 2 and 5). However, Iida does not teach that the diode is connected to a potential-clamped input terminal of at least one functional block. Therefore, Iida fails to disclose or teach a diode connected to a potential-clamped input terminal of at least one of the functional blocks. Thus, Iida does not disclose or teach all the elements of the claimed invention.

Claims 10-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Iida in view of Katsube (U.S. Patent 5,828,119). For at least the following reasons, the examiner's rejection is respectfully traversed.

None of the references disclose or suggest that "the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks" as recited in claim 10. Similar language is found in claims 12 and 14.

As mentioned previously for claims 5, 7, and 9, Iida discloses a diode connected between the gate and the substrate of a pMOS transistor. Iida also discloses that wiring connecting two cells passes through a diode (see Figs.2, 5). However, Iida fails to disclose or suggest that the diode is connected to a potential-claimed input terminal of at least one of the functional blocks. Thus, Iida does not disclose or suggest all the limitations of the claimed invention. Katsube does not over come the limitation of the Iida patent. Therefore, even if combined, the references do not disclose or suggest all the elements of the claimed invention.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 31638US4.

Respectfully submitted,

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